DETAILED ACTION

1. Claims 1-2, 7-8, 15, and 18-20, 22-26, and 29-37 are presented for examination.

2. This action is in response to the Amendment/Response and Affidavit on 10/5/09.

Applicant's arguments have been fully considered but were not found to be persuasive.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 19, 22, 32, and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Kumar et al. (hereinafter Kumar) ("Processor Power Reduction Via Single-ISA Heterogeneous Multi-Core Architectures", IEEE Computer Architecture Letters, Vol. 1, Issue 1, January 2002).

4. Kumar ("Processor Power Reduction Via Single-ISA Heterogeneous Multi-Core Architectures", IEEE Computer Architecture Letters, Vol. 1, Issue 1, January 2002) was cited in the previous office action on 6/26/09 as prior art made of record and not upon. This 102(b) date reference is now being relied upon in the rejection of this office action.

5. As to claim 1, Kumar teaches a computer system (computer system with Single-ISA Heterogeneous Multi-Core Architectures) (see Title and Abstract), comprising:

a plurality of computer processor cores in which at least two differ of the computer processor cores are heterogeneous, and wherein the plurality of computer processor cores execute the same instruction set (Single-ISA Heterogeneous Multi-Core Architecture) (see Title and Abstract); and

a performance measurement and transfer mechanism configured to move a plurality of executing computer processing jobs amongst the plurality of computer processor cores by matching requirements of the plurality of executing computer processing jobs to processing capabilities of the computer processor cores (evaluates the resource requirements of an application and chooses the core that can best meet these requirements) (see Title and Abstract).

6. As to claim 2, Kumar teaches further comprising: at least one of an operating system, hosted on the plurality of computer processor cores, firmware, and special-purpose hardware that includes the performance measurement and transfer mechanism, and the at least one of the operating system, firmware, and special-purpose hardware is configured to provide for a periodic test to determine relative performance of different jobs on different ones of the plurality of computer processor cores (see Abstract).

7. As to claim 19, Kumar teaches wherein the performance measurement and transfer mechanism is configured to transfer the executing computer processing jobs to a new assignment amongst the plurality of computer processor cores, collect performance statistics about execution at the new assignment, and then determine whether to reassign the executing computer processing jobs to different computer processor cores based on the performance statistics collected (see Title and Abstract).

8. As to claim 22, Kumar teaches wherein the determination of whether to reassign the jobs to different computer processor cores also is based on at least one of user-defined or workload-defined metrics (see Title and Abstract).

9. As to claim 32, Kumar teaches wherein the processing capabilities of the computer processor cores are defined by one or more of chip area, available resource, and relative speed of the computer processor cores (see Title and Abstract).

10. As to claim 34, Kumar teaches wherein the performance measurement and transfer mechanism is configured to further re-assign the plurality of executing computer processing jobs amongst the plurality of computer processor cores by repeatedly performing a test to match the requirements of the plurality of executing computer processing jobs to the processing capabilities of the computer processor cores (dynamically chooses the most appropriate core to meet specific performance/throughput and power requirements) (see Abstract).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 7-8, 15, 18, 24, 29-30, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar in view of Calder et al. (hereinafter Calder) (US 2004/0111708 A1).

12. As to claim 7, Kumar teaches a method for operating multiple processor cores, comprising:

obtaining a metric achieved by a plurality of computer processor cores as a function of workloads running on said computer processor cores, wherein the plurality of computer processor cores are on a single semiconductor die, in which at least two computer processor cores differ in processing capability, and wherein the computer processor cores execute the same instruction set (see Title and Abstract); and

transferring individual ones of a plurality of computer processing jobs amongst targeted ones of said plurality of computer processor cores (see Title and Abstract).

13. Kumar does not expressly teach the metric pertains to throughput and that the throughput metric is improved.

14. However, Calder teaches several heterogeneous cores having a single ISA architecture that tracks statistics to optimize run-time performance (lines 1-4 of [0049]; [0055]; claim 51). It would have been obvious to one of ordinary skill in the art to modify Kumar's multi-core processing system such that it would contain the feature of improving metrics of throughput, as taught and suggested in the multi-core processing system of Calder. The suggestion/motivation for doing so would have been to provide the predicted result of improving performance of the system, specifically the run-time performance, for example (lines 1-4 of [0049]; [0055]; claim 51).

15. As to claim 8, Kumar teaches providing for a periodic test to determine relative performance of different jobs on different ones of the computer processor cores (see Abstract).

16. As to claim 15, Kumar (Abstract) and Calder ([0041]; Abstract) teaches further comprising: associating workloads for execution on specific processor cores based on annotations associated with the computer processing jobs. It would be obvious that the choosing of the most appropriate core to meet specific performance and power requirements would involve annotations for the matching because it annotations would provide the means for providing the information needed for the connection/matching of core to requirement.

17. As to claim 18, Kumar is silent in expressly teaching wherein the performance measurement and transfer mechanism is configured to maximize total system throughput. However, Calder teaches several heterogeneous cores having a single ISA architecture that tracks statistics to optimize run-time performance (lines 1-4 of [0049]; [0055]; claim 51). It would have been obvious to one of ordinary skill in the art to modify Kumar's multi-core processing system such that it would contain the feature of improving metrics of throughput, as taught and suggested in the multi-core processing system of Calder. The suggestion/motivation for doing so would have been to provide the predicted result of improving performance of the system, specifically the run-time performance, for example (lines 1-4 of [0049]; [0055]; claim 51).

18. As to claim 24, Kumar does not expressly teach wherein movement of the executing computer processing jobs is constrained to occur only at operating system time slice intervals. However, Calder teaches wherein movement of the executing computer processing jobs is constrained to occur only at operating system time slice intervals ([0049]; 0053]; Abstract). It would have been obvious to one of ordinary skill in the art to modify Kumar's multi-core processing system such that it would contain the feature of wherein movement of the executing computer processing jobs is constrained to occur only at operating system time slice intervals, as taught and suggested in the multi-core processing system of Calder because it would allow for time-slicing scheduling, which is a known strategy for achieving the benefits of power-savings.

19. As to claim 29, Kumar teaches a method for operating multiple processor cores, comprising:

obtaining a metric that identifies throughput achieved by computer processor cores on a single semiconductor die as a function of workloads running on said computer processor cores (see Title and Abstract); and

assigning a plurality of computer processing jobs amongst a plurality of computer processor cores based on the throughput metric, wherein at least two of the computer processor cores differ in size or complexity (cores of varying complexity) but execute the same instruction set (see Title and Abstract);

transferring the computer processing jobs to a new assignment amongst the plurality of computer processor cores (see Title and Abstract);

collecting statistics about execution performance of the computer processing jobs at the new assignment (performance and power statistics) (see Title and Abstract);

determining whether to reassign (choosing dynamically) the computer processing jobs to different computer processor cores based on the statistics collected (see Title and Abstract); and

utilizing relative performances of the computer processing jobs on different types of computer processor cores based on statistics collected (see Title and Abstract).

20. Kumar does not expressly teach the metric pertains to throughput and that the throughput metric is improved.

21. However, Calder teaches several heterogeneous cores having a single ISA architecture that tracks statistics to optimize run-time performance (lines 1-4 of [0049]; [0055]; claim 51). It would have been obvious to one of ordinary skill in the art to modify Kumar's multi-core

processing system such that it would contain the feature of improving metrics of throughput, as taught and suggested in the multi-core processing system of Calder. The suggestion/motivation for doing so would have been to provide the predicted result of improving performance of the system, specifically the run-time performance, for example (lines 1-4 of [0049]; [0055]; claim 51).

22. In addition, Kumar in view of Calder does not explicitly teach building a data structure for the relative performances of jobs.

23. However, one of ordinary skill in the art would know that it is well known to use data structures to contain computing data. It would have been obvious to one of ordinary skill in the art to build a data structure for Kumar in view of Calder's recorded and tracked relative performances of core jobs so that the data can be organized and utilized for computer processing.

24. As to claim 30, Kumar teaches wherein the determination of whether to reassign the jobs to different computer processor cores also is based on at least one of user-defined or workload-defined metrics (see Title and Abstract).

25. As to claim 37, Calder teaches wherein the throughput metric indicates total system throughput, and wherein assigning maximizes the total system throughput, as indicated by the throughput metric ([0138]; [0055]; claim 51).

26. Claims 20 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar.

27. As to claim 20, Kumar teaches a computer system (computer system with Single-ISA Heterogeneous Multi-Core Architectures) (see Title and Abstract), comprising:

a plurality of computer processor cores in which at least two differ in processing performance, and wherein the plurality of computer processor cores execute the same instruction set (computer system with Single-ISA Heterogeneous Multi-Core Architectures) (see Title and Abstract); and

a performance measurement and transfer mechanism configured to move a plurality of executing computer processing jobs amongst the plurality of computer processor cores based on a measured throughput metric (matches the applications to the different cores based on a given performance/throughput requirement or goal) (see Title and Abstract),

wherein the performance and transfer mechanism is configured to swap execution (swaps when choosing most appropriate core during execution) of the executing computer processing jobs between the computer processor cores for a period of time (during execution, etc.), monitor resulting performance of relative performances of jobs on different types of computer processor cores (Abstract).

28. Kumar does not explicitly teach building a data structure for the relative performances of jobs. However, one of ordinary skill in the art would know that it is well known to use data structures to contain computing data. It would have been obvious to one of ordinary skill in the

art to build a data structure for Kumar's tracked relative performances of core jobs so that the data can be organized and utilized for computer processing.

29. As to claim 33, Kumar teaches associating workloads for execution on specific processor cores based on annotations associated with the computer processing jobs (Abstract). It would be obvious that the choosing of the most appropriate core to meet specific performance and power requirements would involve annotations for the matching because it annotations would provide the means for providing the information needed for the connection/matching of core to requirement.

30. Claims 23 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar in view of Calder, and further in view of Nagae (US 6,006,248).

31. Nagae was cited in the previous office action.

32. As to claim 23, Kumar in view of Calder is silent in teaching wherein the performance/throughput metric comprises a number of instructions per second. However, Nagae teaches a job application distribution system among a plurality of processors, wherein CPU performance is evaluated and may comprise of the number of instructions per second (col. 18,

lines 35-43). One of ordinary skill in the art would have known to modify Kumar in view of Calder's performance/throughput metric such that it would comprise of the number of instructions per second because it would provide the predicted result of utilizing a standard and well-known unit that is common to the user.

33. As to claim 31, it is rejected for the same reasons as stated in the rejections of claims 23.

34. Claims 25-26 and 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar in view of Paker et al. (hereinafter Paker) ("A heterogeneous multi-core platform for low power signal processing in systems-on-chip", 2002).

35. As to claim 25, Kumar teaches a method for operating multiple processor cores, comprising:

assigning a plurality of computer processing jobs amongst a plurality of computer processor cores, wherein at least two of the computer processor cores differ in complexity (heterogeneous/different cores differ in complexity) but execute the same instruction set (see Title and Abstract), and

wherein assigning the plurality of computer processing jobs amongst the plurality of computer processor cores comprises matching requirements of the computer processing jobs to

processing capabilities of the computer processor cores based on the sizes or complexities of the computer processor cores (see Title and Abstract).

36. Kumar does not teach that its heterogeneous multi-core processor specifically refer to the cores differing in size.

37. However, Paker teaches a heterogeneous multi-core processing system such that cores differ in size and complexity so that the processing is both flexible and energy efficient (Abstract; last paragraph of page 73; first paragraph of page 74). Kumar and Paker are analogous art because they are in the same field of endeavor of multi-core processing and both are attempting to solve the same problem of improving processing performance. Thus, one of ordinary skill in the art would have known to modify Kumar's heterogeneous multi-core processing system such that it would include the feature of having its cores differ in size and complexity, as taught and suggested in Paker's heterogeneous multi-core processing system. The suggestion/motivation for doing so would have been to provide the predicted result of increased flexibility/customization through the differing cores, etc. (Paker - Abstract; last paragraph of page 73; first paragraph of page 74).

38. As to claim 26, Kumar teaches providing for a periodic test to determine relative performance of different jobs on different ones of the computer processor cores (see Abstract).

39. As to claim 35, Kumar teaches associating workloads for execution on specific processor cores based on annotations associated with the computer processing jobs (Abstract). It would be obvious that the choosing of the most appropriate core to meet specific performance and power

requirements would involve annotations for the matching because it annotations would provide the means for providing the information needed for the connection/matching of core to requirement.

40. As to claim 36, Kumar teaches repeatedly performing a test to match requirements of the computer processing jobs to the processing capabilities of the computer processor cores; and reassigning the plurality of computer processing jobs amongst the plurality of computer processor cores based on the repeated tests (dynamically chooses the most appropriate core to meet specific performance/throughput and power requirements) (see Abstract).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

41. Claims 1-2, 7-8, 15, 18-19, 22, 24, and 32-34 are rejected under 35 U.S.C. 102(a) as being anticipated by Calder et al. (hereinafter Calder) (US 2004/0111708 A1).

42. As to claim 1, Calder teaches a computer system (Abstract), comprising:

a plurality of computer processor cores in which at least two differ of the computer processor cores are heterogeneous, and wherein the plurality of computer processor cores

execute the same instruction set (single ISA architecture that has several heterogeneous cores) (lines 1-4 of [0049]); and

a performance measurement and transfer mechanism configured to move (switching) a plurality of executing computer processing jobs amongst the plurality of computer processor cores by matching requirements of the plurality of executing computer processing jobs to processing capabilities of the computer processor cores ([0049]; Abstract).

43. As to claim 2, Calder teaches further comprising: at least one of an operating system, hosted on the plurality of computer processor cores, firmware, and special-purpose hardware that includes the performance measurement and transfer mechanism, and the at least one of the operating system, firmware, and special-purpose hardware is configured to provide for a periodic test to determine relative performance of different jobs on different ones of the plurality of computer processor cores (operating system) ([0108]; [0205]).

44. As to claim 7, Calder teaches a method for operating multiple processor cores, comprising:

obtaining a throughput metric that identifies throughput achieved by a plurality of computer processor cores as a function of workloads running on said computer processor cores, wherein the plurality of computer processor cores are on a single semiconductor die, in which at least two computer processor cores differ in processing capability, and wherein the computer

processor cores execute the same instruction set (single ISA architecture that has several heterogeneous cores) (lines 1-4 of [0049]; [0055]; claim 51); and

transferring (switching) individual ones of a plurality of computer processing jobs amongst targeted ones of said plurality of computer processor cores to improve a throughput metric ([0049]; see claim 51; Abstract).

45. As to claim 8, Calder teaches providing for a periodic test to determine relative performance of different jobs on different ones of the computer processor cores (lines 1-4 of [0049]; [0055]).

46. As to claim 15, Calder teaches further comprising: associating workloads for execution on specific processor cores based on annotations associated with the computer processing jobs ([0041]; Abstract).

47. As to claim 18, Calder teaches wherein the performance measurement and transfer mechanism is configured to maximize total system throughput ([0049]; see claim 51; Abstract).

48. As to claim 19, Calder teaches wherein the performance measurement and transfer mechanism is configured to transfer the executing computer processing jobs to a new assignment

amongst the plurality of computer processor cores, collect performance statistics about execution at the new assignment, and then determine whether to reassign the executing computer processing jobs to different computer processor cores based on the performance statistics collected ([0049]; see claim 51; Abstract).

49. As to claim 22, Calder teaches wherein the determination of whether to reassign the jobs to different computer processor cores also is based on at least one of user-defined or workload-defined metrics ([0041]).

50. As to claim 24, Calder teaches wherein movement of the executing computer processing jobs is constrained to occur only at operating system time slice intervals ([0049]; 0053]; Abstract).

51. As to claim 32, Calder teaches wherein the processing capabilities of the computer processor cores are defined by one or more of chip area, available resource, and relative speed of the computer processor cores ([0049]; [0055]).

52. As to claim 33, it is rejected for the same reasons as stated in the rejection of claim 15.

53. As to claim 34, Calder teaches wherein the performance measurement and transfer mechanism is configured to further re-assign the plurality of executing computer processing jobs

amongst the plurality of computer processor cores by repeatedly performing a test to match the requirements of the plurality of executing computer processing jobs to the processing capabilities of the computer processor cores ([0049]; [0054]; [0055]; see claim 51; Abstract).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

54. Claims 20-21, 29-30, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calder.

55. As to claim 20, Calder teaches a computer system (Abstract), comprising:

a plurality of computer processor cores in which at least two differ in processing performance, and wherein the plurality of computer processor cores execute the same instruction set (single ISA architecture that has several heterogeneous cores) (lines 1-4 of [0049]; [0055]); and

a performance measurement and transfer mechanism configured to move a plurality of executing computer processing jobs amongst the plurality of computer processor cores based on a measured throughput metric ([0049]; [0054]; [0055]; see claim 51; Abstract),

wherein the performance and transfer mechanism is configured to swap execution of the executing computer processing jobs between the computer processor cores for a period of time, monitor resulting performance (tracking statistics), and recording relative performances of jobs on different types of computer processor cores ([0049]; see claim 51; Abstract).

56. Calder does not explicitly teach building a data structure for the relative performances of jobs. However, one of ordinary skill in the art would know that it is well known to use data structures to contain computing data. It would have been obvious to one of ordinary skill in the art to build a data structure for Caldor's recorded and tracked relative performances of core jobs so that the data can be organized and utilized for computer processing.

57. As to claim 21, Calder teaches wherein the jobs are reassigned based on the relative performances, by assigning jobs that benefited most from large complex cores to said large complex cores (lines 1-4 of [0049]; [0055]).

58. As to claim 29, Caldor teaches a method for operating multiple processor cores, comprising:

obtaining a throughput metric that identifies throughput achieved by computer processor cores on a single semiconductor die as a function of workloads running on said computer processor cores (single ISA architecture that has several heterogeneous cores) (lines 1-4 of [0049]; [0055]); and

59. assigning a plurality of computer processing jobs amongst a plurality of computer processor cores based on the throughput metric, wherein at least two of the computer processor cores differ in size or complexity (Being heterogeneous and different cores, Calder's cores differ in complexity) but execute the same instruction set (single ISA architecture that has several heterogeneous cores) (lines 1-4 of [0049]; [0055]);

transferring (switching) the computer processing jobs to a new assignment amongst the plurality of computer processor cores ([0049]; Abstract);

collecting statistics about execution performance of the computer processing jobs at the new assignment ([0049]; see claim 51; Abstract);

determining whether to reassign the computer processing jobs to different computer processor cores based on the statistics collected ([0049]; Abstract); and

60. Calder does not explicitly teach building a data structure for the relative performances of jobs. However, one of ordinary skill in the art would know that it is well known to use data structures to contain computing data. It would have been obvious to one of ordinary skill in the art to build a data structure for Caldor's recorded and tracked relative performances of core jobs so that the data can be organized and utilized for computer processing.

61. As to claim 30, Calder teaches wherein the determination of whether to reassign the jobs to different computer processor cores also is based on at least one of user-defined or workload-defined metrics ([0041]).

62. As to claim 37, Calder teaches wherein the throughput metric indicates total system throughput, and wherein assigning maximizes the total system throughput, as indicated by the throughput metric ([0138]; [0055]; claim 51).

63. Claims 23 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calder in view of Nagae (US 6,006,248).

64. As to claims 23 and 31, Calder is silent in teaching wherein the performance/throughput metric comprises a number of instructions per second. However, Nagae teaches a job application distribution system among a plurality of processors, wherein CPU performance is evaluated and may comprise of the number of instructions per second (col. 18, lines 35-43). One of ordinary skill in the art would have known to modify Calder's performance/throughput metric such that it would comprise of the number of instructions per second because it would provide the predicted result of utilizing a standard and well-known unit that is common to the user.

65. Claims 25-26 and 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calder in view of Paker et al. (hereinafter Paker) ("A heterogeneous multi-core platform for low power signal processing in systems-on-chip", 2002).

66. As to claim 25, Calder teaches a method for operating multiple processor cores (multi-core) ([0049]), comprising:

assigning a plurality of computer processing jobs amongst a plurality of computer processor cores, wherein at least two of the computer processor cores differ in complexity (heterogeneous multi-core) but execute the same instruction set (single ISA architecture that has several heterogeneous cores) (lines 1-4 of [0049]; [0055]), and

wherein assigning the plurality of computer processing jobs amongst the plurality of computer processor cores comprises matching requirements of the computer processing jobs to processing capabilities of the heterogeneous computer processor cores.

67. Being heterogeneous and different cores, Calder's cores differ in complexity.

68. Calder does not teach that its heterogeneous multi-core processor specifically refer to the cores differing in size.

69. However, Paker teaches a heterogeneous multi-core processing system such that cores differ in size and complexity so that the processing is both flexible and energy efficient (Abstract; last paragraph of page 73; first paragraph of page 74). Calder and Paker are analogous art because they are in the same field of endeavor of multi-core processing and both are attempting to solve the same problem of improving processing performance. Thus, one of ordinary skill in the art would have known to modify Calder's heterogeneous multi-core

processing system such that it would include the feature of having its cores differ in size and complexity, as taught and suggested in Paker's heterogeneous multi-core processing system. The suggestion/motivation for doing so would have been to provide the predicted result of increased flexibility/customization through the differing cores, etc. (Abstract; last paragraph of page 73; first paragraph of page 74).

70. As to claim 26, Calder teaches providing for a periodic test to determine relative performance of different jobs on different ones of the computer processor cores (lines 1-4 of [0049]; [0055]).

71. As to claim 35, Calder teaches further comprising: associating workloads for execution on specific processor cores based on annotations associated with the computer processing jobs ([0041]; Abstract).

72. As to claim 36, Calder teaches repeatedly performing a test to match requirements of the computer processing jobs to the processing capabilities of the computer processor cores; and reassigning the plurality of computer processing jobs amongst the plurality of computer processor cores based on the repeated tests ([0049]; [0054]; [0055]; see claim 51; Abstract).

Response to Arguments

73. Claims 1-2, 17, 19, 22, 32, and 34 are based upon the statutory bar rejection under 35 USC 102(b) results in a statutory bar to obtaining a patent.

74. The declaration under 37 CFR 1.132 filed 5/14/10 is insufficient to overcome the rejection of claims 1-2, 17, 19, 22, 32, and 34 are based upon the rejection under 35 USC 102(b) over Kumar as set forth in the last Office action because: the evidence is not found to be persuasive because it does not rely on facts, but instead, relies on mere recollection that the first submission of the paper (the Multi-Core Architecture Paper reflected in Exhibit A) was believed to have been submitted in March 2003 (see paragraph 14 of the declaration). The Examiner advises the Applicant that an affidavit from the publisher, IEEE Computer Society, confirming the error would be sufficient evidence and would be found to be persuasive.

75. Applicant argues that Calder is not valid prior art because the '105 Provisional Application and the '106 Provisional Application that Calder claims the benefit of do not contain the content of Calder relied upon by the Office Action. Neither of the provisional applications disclose any of the following concepts: heterogeneous cores, multi-core architecture, or guiding each phase of program execution to a specific core.

76. '106 Provisional Application teaches simultaneous multithreading (SMT) (page 5, section 2 Motivation, etc.) and one of ordinary skill in the art would know that a multi-core processor would provide the means for the SMT processing. Thus, one of ordinary skill in the art would know that '105 Provisional Application (pages 1-2, etc.) and '106 Provisional Application (page 5, section 2 Motivation, etc.) teach and suggest the disclosure of the Calder specification.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- **Kohn et al. (US 2003/0088610 A1)** discloses resource allocation of a multi-core multi-thread processor.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KENNETH TANG whose telephone number is (571)272-3772. The examiner can normally be reached on 9:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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